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09/778,233	02/06/2001	Lane Hauck	CYPR-CD00205.US.P	5757

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EXAMINER	
CASIANO, ANGEL L	

ART UNIT	PAPER NUMBER
2182	6

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/778,233	Applicant(s) HAUCK ET AL.	
	Examiner Angel L. Casiano	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The present Office Action is in response to Amendment dated 06 November 2003.

2. Claims 1-27 are pending in the present application.

Drawings

3. Previous Objections to the Drawings have been overcome with the corrections filed in the present Amendment.

4. The corrected drawings were received on 12 November 2003. These drawings are accepted by the Examiner.

Specification

5. Previous Objection to the Specification has been overcome with the corrections included in the present Amendment.

Claim Rejections - 35 USC § 112

6. In the previous Office action, claims 6, 7 and 23 were rejected under 35 U.S.C. 112, second paragraph. These rejections have been overcome with the corrections filed in the present Amendment.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art [AAPA], in view of Gates [US 5,826,068].

Regarding claim 1, applicant admits to the prior art method including sending a "READ command" (see page 1, lines 26-27) from a memory controller (see page 2, line 2) chip to a serial peripheral interface (SPI) device (see page 1, lines 15-17) over an SPI interface (see page 1, line 10). However, applicant does not admit to the prior art method including a series of serial clock cycles. Nonetheless, Gates explicitly teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and further suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, lines 1 and 12; col. 48, lines 27-29). Nonetheless, the cited references do not teach automatically detecting the presence of non-zero values coming from the SPI device through a D-IO pin during a series of serial clock cycles. The cited art does not include an indication that the SPI device has memory addresses up to nine or sixteen bits, as claimed (see steps (d), (e)). However, it should be noted that Gates teaches a pin (see col. 47, lines 6-11) as part of its method for automatically detecting memory size. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings

of Gates and applicant's knowledge to prior art because Gates' method, including a bi-directional pin, when incorporated into the admitted prior art, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54). Furthermore, although the cited art does not specify ("first", "second", "third", "fourth") serial clock cycles, the admission of prior art [AAPA] suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to combine the admitted method [AAPA] in order to include a pin, as disclosed by Gates, for the purposes of having an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claims 2 and 3, the cited art does not teach a first and second SPI device having up to 512 bytes (claim 2) and 64 kilobytes (claim 3) of memory, respectively. Nonetheless, Gates teaches detecting the memory size of an EEPROM (see col. 42, lines 17-22). Although Gates does not specify 512 bytes or 64 kilobytes, it would have been obvious to one of ordinary skill in the art that the reference is capable of detecting different memory sizes (see col. 42, lines 17 and 22). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention that the claimed memory sizes constitute specific examples of available EEPROM memory sizes. Furthermore, one of ordinary skill in the art at the time of the invention would have been motivated to combine applicant's knowledge and the cited reference, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

Considering claim 4, the cited art does not expressly teach a sensing circuit within a memory controller chip. Nonetheless, applicant admits to a memory controller (see page 1, line 13) chip in a method. In addition, Gates explicitly teaches a sensing circuit for automatically detecting memory size (see col. 41, line 10; Fig. 13, "1370"). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a pin, when incorporated into admitted prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54).

As for claim 5, applicant's admission of prior art [AAPA] includes a memory controller chip (see page 1, line 13) driving a serial clock signal (inherent, see page 2, lines 14-15) between a controller chip and an SPI device (see page 1, lines 13-17).

Considering claim 6, the admission of prior art [AAPA] does not explicitly cite an SPI device having a non-zero value located at its first address byte. Nonetheless, Gates teaches detecting a non-zero value (see col. 42, lines 20-21) at a first memory address line, as part of a method for automatically detecting memory size of an SPI device (see "EEPROM", col. 42, line 22). Accordingly, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the admitted prior art and the cited reference in order to provide reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) for a method of automatically detecting memory size.

As for claim 7, applicant admits to the prior art method including a memory controller (see page 1, line 13) chip and a serial peripheral interface (SPI) device (see page 1, lines 15-17) communicating over an SPI interface (see page 1, line 10). In addition, Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, line 12; col. 48, lines 27-29). The prior art disclosures do not specify the memory controller chip as having three controller pins. Nevertheless, the admitted prior art [AAPA] teaches that the SPI interface (bus) is a "3-wire" interface (see page 2, lines 12-13), but taking into account all the necessary connections, it would be a "5-wire" interface (see page 3, line 5). It should be noted, however, that Gates teaches a pin ("bi-directional", see col. 47, lines 6-11) in a method of automatically detecting memory size. In another aspect of the claim, the prior art method does not explicitly include SI and SO pins coupled to a pulldown resistor. However, Gates teaches an SPI device having a resistor driving a pin to a logic "0" level (see col. 42, lines 7-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) since it reduces the number of necessary pins. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claim 8, applicant's admission of prior art [AAPA] does not specify ("first", "second", "third", "fourth") serial clock cycles, but suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles (inherent, see col. 47, line 12; col. 48, lines 27-29). In addition, Gates explicitly teaches the indication of absence of an SPI device (see col. 42, line 5).

As for claim 9, Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, line 12; col. 48, lines 27-29). Nonetheless, the cited references do not explicitly teach automatically detecting the presence of zero or non-zero values coming from the SPI device through a D-IO pin during a series of serial clock cycles. The cited art does not include an indication that the SPI device has memory addresses up to twenty-four bits, as claimed. However, it should be noted that Gates teaches a pin (see col. 47, lines 6-11) in a method of automatically detecting memory size. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54). Furthermore, although the cited art does not specify ("first", "second", "third", "fourth", "fifth") serial clock cycles, the admission of prior art suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to

include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claim 10, the prior art method does not explicitly include SI and SO pins coupled to a pulldown resistor. However, Gates teaches an SPI device having a resistor driving a pin to a logic "0" level (see col. 42, lines 7-9). It would have been obvious for one of ordinary skill in the art at the time the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) since it reduces the number of necessary pins. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claims 11-17, these constitute the SPI circuit for the method disclosed in claims 1-10. The prior art cited teaches or suggests all the limitations corresponding to the method claims 1-10. Claims 11-17 are therefore rejected under the same rationale.

As for claims 18-27, these are oriented to the system including instructions that when executed (see claim 18, lines 26-27), implement the method disclosed in claims 1-10. The prior art cited

teaches or suggests all the limitations corresponding to the method claims 1-10. Accordingly, the present claims are rejected under the same rationale.

Response to Arguments

9. Applicant's arguments filed 06 November 2003 have been fully considered but they are not persuasive.

10. Regarding applicant's arguments on Page 19, first paragraph, these do not seem to apply to the present application, since previous Office action was mailed on 07 August 2003 (not 02 May 2003). In addition, claims 1-27 are pending in the present application (not 1-15).

In page 25, applicants assert that claims 10-27 are allowable, since these depend from independent claim 18. Examiner respectfully submits that only claims 19-27 depend from claim 18.

11. In the remarks, applicants argued in substance that the combination of references does not teach or suggest detecting the memory size of an SPI (claim 1). Examiner respectfully disagrees. In another aspect of the claim, applicants argue that the prior art does not explicitly teach "*examining the signals received from the SPI device over a single D-I/O pin*". Examiner agrees. Nonetheless, the combination of references does teach or suggest the limitations corresponding to the claim (see Rejections). In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore, the test for obviousness under 35 U.S.C. 103 is not the express suggestion of the claimed invention in any or all of the references but what the references taken collectively would suggest. See *In re Conrad*, 169 USPQ 170 (CCPA 1971).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Chiang et al. [US 6,370,642 B1] teaches a boot ROM **size detection circuit**.
- Reohr, Jr. et al. [US 6,298,006 B1] teaches **method** and **apparatus** to **automatically determine** the **size** of an external **EEPROM**.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 9:30-6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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alc
February 7, 2004